

Figure 1A

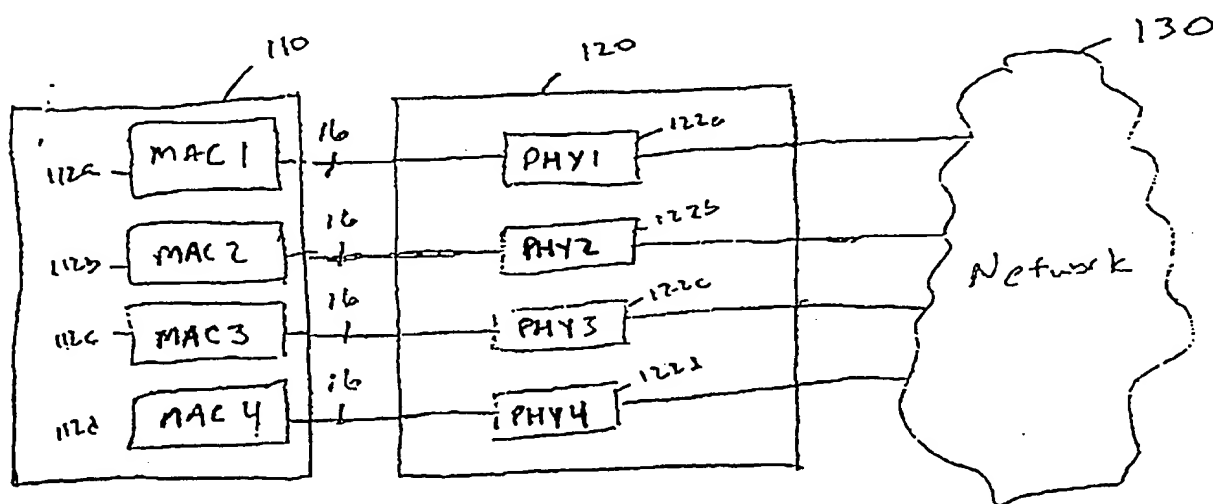


Figure 1B

Hand-drawn block diagram showing the interface between a MAC (Media Access Control) block and a PHY (Physical Layer) block. The MAC block is on the left, and the PHY block is on the right. A 125 MHz clock signal is connected to the PHY block.

**MAC Block Signals:**

- TXC
- TX-EN
- TX-ER
- TXD[3:0]
- CRS
- COL
- RXC
- RXD[3:0]
- RX-DV
- RX-ER
- MAC

**PHY Block Signal:**

- PHY

**Handwritten Labels:**

- 200 (above TXC)
- 202 (above PHY)
- 210 (above TX-EN)
- 212 (above TX-ER)
- 214 (above TXD[3:0])
- 215 (above CRS)
- 218 (above COL)
- 220 (above RXC)
- 222 (above RXD[3:0])
- 224 (above RX-DV)
- 226 (above RX-ER)
- 228 (above MAC)

Figure 2

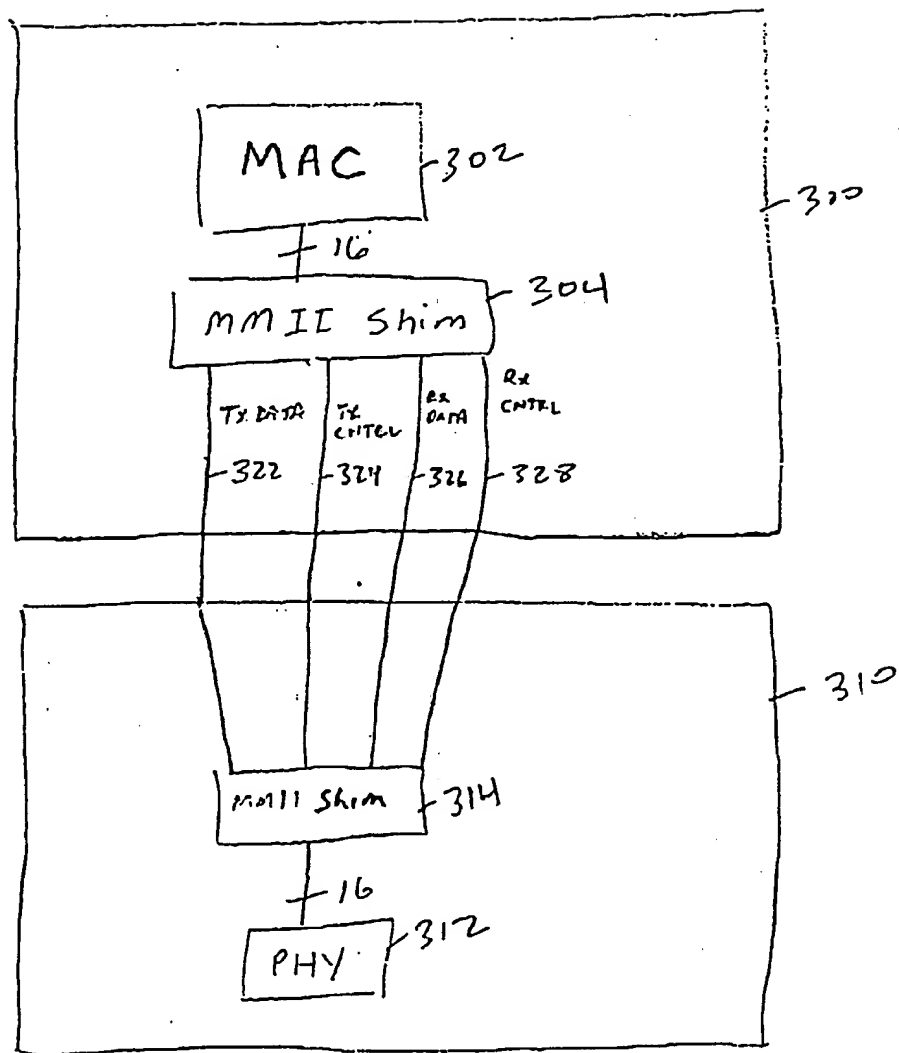


Figure 3

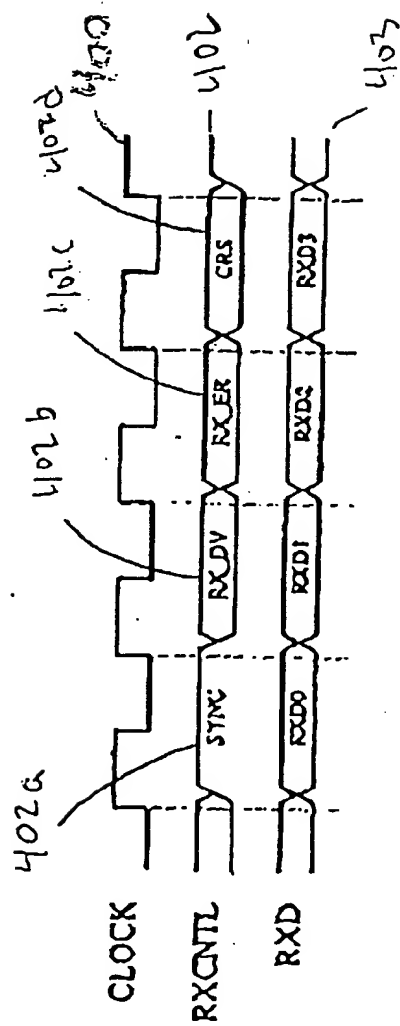


Figure 4

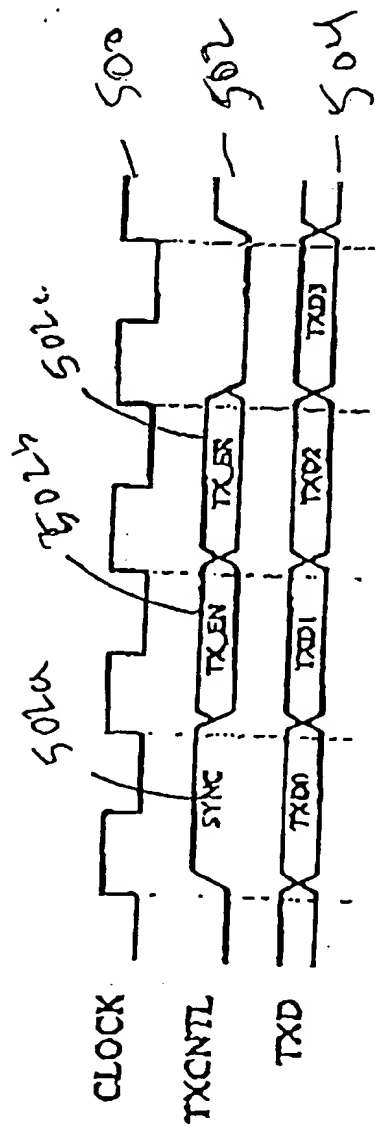


FIGURE 5

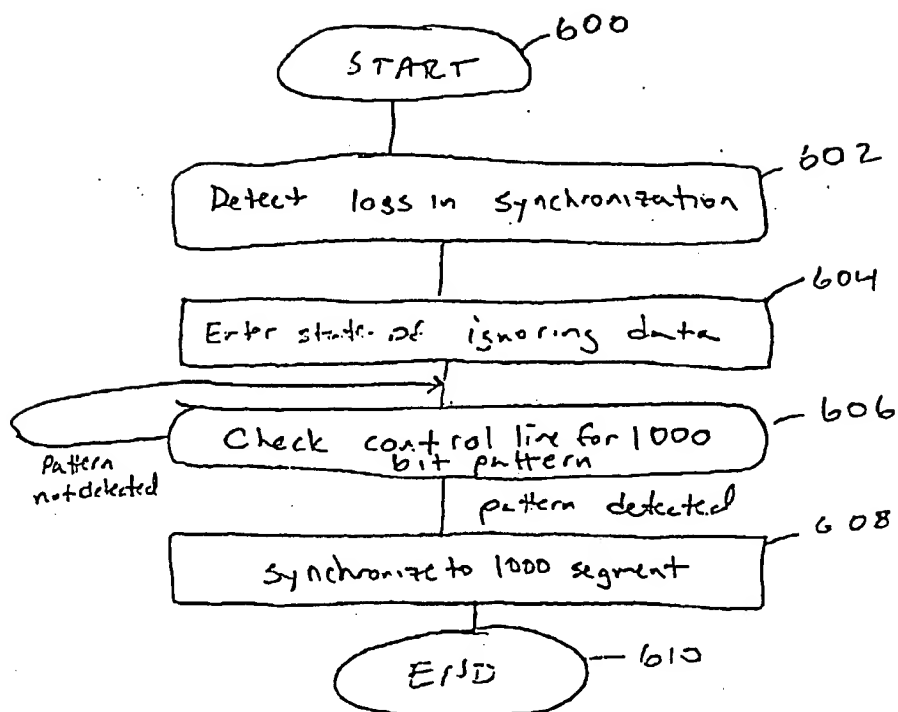


Figure 6

